DSP FOR FPGAS SHORT COURSE

steepest ascent

DSP for FPGAs

In the next 5 years we can anticipate more wireless and digital communication standards, pervasive computing and widespread availability of data on the move. Therefore the growing requirements for processing speeds of the order of 10-100 billions of operations per second, the need for rapid prototyping and software definable architectures will further penetration of FPGAs into the DSP communication market.

The DSP for FPGAs course will review DSP fundamentals from the perspective of implementation within the FPGA fabric. Particular emphasis will be given to highlighting the cost, with respect to both resources and performance, associated with the implementation of various DSP techniques and algorithms. As this course provides sound grounding in the rudiments of DSP theory and algorithms it is suitable for engineers from a wide range of application backgrounds.

This course has been successfully presented in the USA at the University of California, Los Angeles (UCLA) twice a year since 2002 and in the UK at the Institute for System Level Integration (ISLI) each year since 2004. The course has also been presented on-site at a number of companies throughout Europe and the USA.

COURSE AIM

To present theory, algorithms, design techniques and actual practicalities of the implementation of DSP algorithms and digital communications architectures using FPGA technology.

AUDIENCE

Analogue, RF, digital, DSP or FPGA/ASIC engineers who are interested in knowing the relevant design strategies and philosophies for implementing algorithms and applications on FPGAs may find the course beneficial.

COURSE PRESENTATION

This is an intensive 4 day course which will educate using a comprehensive set of notes on DSP for FPGAs. Key points will be lectured upon with derivations and technical details provided in the course notes for later self study. Following each lecture, hands-on lab sessions will be run using Xilinx FPGA hardware and software.

The course format is:

- 50% Lectures
- 40% Hands-on Labs (FPGA hardware and software)
- 10% Demonstrations

ACHIEVABLE SKILLS

On successful completion of the course, attendees will be able to:

- Understand the current and relevant DSP applications for FPGAs
- When to use an FPGA or a DSP processor or both
- Arithmetic issues - How to implement multiplies and adds - efficiently
- The impact of rounding versus truncation
- Dealing with overflow and underflow scenarios
- Advanced Arithmetic- square roots and divides
- Design techniques for minimizing sample wordlengths
- Efficient FIR (Finite Impulse Response) filter design and implementation
- The use of IIR (Infinite Impulse Response) filters in DSP for FPGA applications
- The importance of retiming, pipelining, and multi-channel filters
- The cost and relevance of special filters such as CIC (Cascade Integrate-Comb) filters
- The requirements and implementation of adaptive filtering algorithms
- The implementation of IF modulation and demodulation techniques
- Why and how to implement Numerically Controlled Oscillators (NCOs)
- Techniques for synchronisation & digital communications timing recovery
- System architecture and implementation of direct Digital Down Converter (DDC)
- DSP/FPGA components to implement a QAM (Quadrature Amplitude Modulator) transceiver
- How to efficiently implement multi-channel filters for 3G applications
- Design strategies for implementation of Orthogonal Frequency Division Multiplexing (OFDM)
- Using the QR algorithms for adaptive equalisation and beamforming
- The application of SOC Design methodologies within FPGAs
- Use Embedded Processors within FPGAs to implement DSP algorithms

PRE-REQUISITES

This course has been carefully designed to present the complex mathematical theory often associated with DSP in an intuitive and straightforward style to a wide audience of scientists, engineers and project managers. The following prior experience is useful but not essential: (i) Fundamentals of DSP; (ii) Basic communication systems; (iii) Bachelor level mathematics.

COURSE MATERIALS

All participants will receive more than 1200 pages of notes in 6 professionally bound volumes:

1. Introductory DSP Class Notes
2. Advanced DSP Class Notes
3. DSP Communications Class Notes
4. Advanced Communications Class Notes
5. DSP FPGA Class Notes
6. DSP FPGA Workbook

The notes provided form a superset of the materials presented on the course and will allow further in depth study of DSP after the course.

MULTIMEDIA CD

Each attendee will receive a copy of a multimedia CD featuring:

1. Hypertext of all printed notes
2. Integrated multimedia presentations
3. More than 100 DSP audio demonstrations
4. More than 300 DSP demos
5. DSP Simulation Software Support

LABORATORY SESSIONS

The laboratory sessions will feature the entire software design flow from concept, to bit true simulation, to actual hardware implementation on a Xilinx XUP Virtex-II Pro development kit which consisting of the Xilinx XC2VP30 FPGA.

SYLLABUS

DSP for FPGA Technology & Application Review

- DSP for FPGA applications
- Wordlength issues- possibility of variable wordlengths
- Design for applications sampling at > 100MHz
- FPGA applications examples: 3G, 802.16, cdma2000
- FPGAs, DSP processors, ASICs- what to use when and where
- Linear algebra- matrices, vectors
- Calculating the matrix inverse and DSP requirements

FPGA Technology

- The Xilinx DSP for FPGA technology roadmap
- Clocking rates, data rates and sample rates
- Bits, Slices, Configurable Logic Blocks & Multipliers
- MIPs and MACs performance ratings
- FPGA families and sources
- Case Study- Virtex 4 and DSP48 slices
- Review of an HDL design flow from algorithm to implementation

Arithmetic Fundamentals

- 2's complement Fixed point arithmetic
- Adders, multipliers and introducing division and square root operations
- Wordlength issues and Fixed point arithmetic
- Overflow/ Underflow and Truncation/ Rounding issues
- Complex arithmetic (real and imaginary) requirements for DSP
- The role of arithmetic approximation algorithms and CORDICs

Digital Filtering for FPGAs

- Symmetric/ Linear Phase Filters- Xilinx efficiency and optimisation
- Upsampling/ Interpolation and Downsampling/ Decimation
- Trade-offs with wordlength, sampling rate and filter lengths
- Retiming techniques
- Cut-set delay for transpose and systolic FIR filters
- Half-band, moving average, comb filters and CIC filters
- Multichannel filter implementation
- Polyphase filter implementation

Adaptive Filtering for FPGAs

- The issues from numerical feedback and how to deal with them
- The LMS (Least Mean Square) algorithm
- LMS implementation and application
- The RLS (Recursive Least Squares) algorithm
- RLS implementation -the QR algorithm- Classical linear algebra
- Numerical integrity and stability issues

QAM (Quadrature Amplitude Modulation) Systems

- The DSP enabled IF Radio architecture (software radio)
- Design of Numerically Controlled Oscillators (NCOs)
- Design of transmit and receive matched digital filters
- Carrier timing recovery, and symbol synchronisation techniques
- Constellations, phase rotations, and test scenarios
- Spread spectrum strategies and requirements

FPGA System Level DSP Applications

- 3G oversampled multichannel filters
- Bluetooth compatible Direct Digital Downconverter (DDC) design
- Adaptive LMS based equalisation for wireline applications
- Adaptive QR algorithm for wireless digital beamforming
- Design of NCO, FIR filter for Generic QAM transmitter

Embedded Processors for FPGAs

- Embedded Systems
- System-on-Chip (SOC) design methodologies and design flows
- On-Chip Network (OCN) topologies and standards
- System profiling and hardware acceleration
- Xilinx Platform Studio (XPS)
- Case Study- Xilinx PicoBlaze, MicroBlaze and Power PC Embedded Processors

MORE DETAILS

Should you have any further questions about this or any other Steepest Ascent course, or you are interested in an on-site presentation please contact:

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